PATENT SPECIFICATION

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1 266 962

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(54) ANALOGUE TO DIGITAL CONVERTER

(71) We, MICRO CONSULTANTS LIMITED, a British Company, of 53, Taunton Lane, Coulsdon, Surrey, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an analogue to digital converter suitable for operating at very high speed.

According to the present invention there is provided an analogue to digital converter comprising a plurality of stages, each stage including a full wave rectifier having first and second input terminals and first and second output terminals, a detector connected between said first and second input terminals, and in each stage except the first, a first and a second constant current source connected respectively to said first and second input terminals, whereby when the converter is connected to an analogue current, the analogue current flows in the full wave rectifier of the first stage between first and second stages, the respective detector providing a logic output when the current flows in one direction through the full wave rectifier and a logic zero when the current flows in the opposite direction through the full wave rectifier to differentiate between an analogue current of greater or less than a predetermined level.

The first and second constant current generators for each stage may be arranged to provide currents of magnitude one half of the magnitude of a predetermined maximum current which is fed to the stage, the current being subtracted from the input current, the magnitude of the currents from said first and second constant current generators for each stage subsequent to the second providing currents equal to one half the magnitude of the current provided by the first and second constant current generators of the previous stage and first and second constant generators of the second stage provide current equal to one half the maximum input current to the converter.

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Each stage of the converter may be provided with a differential amplifier circuit, the output terminals of which are connected to said first and second input terminals of the full wave rectifier and the input terminals of which are connected to the output terminals of the full wave rectifier of the previous stage, which amplifier is arranged to provide an output current from the output terminals of the full wave rectifier which varies linearly between a maximum stage input level, zero and back to maximum as the stage input current varies linearly between maximum and zero.

Constructional embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:—

Figure 1 shows a block diagram of a three stage converter in accordance with the present invention;

Figure 2 shows a graph of the variation of currents occurring in the block diagram of Figure 1,

Figure 3 shows a block diagram of an alternative arrangement for a three stage converter in accordance with the invention.

Figure 4 shows a simplified circuit diagram of one stage of the converter of Figure 3.

Figure 5 shows the current transfer characteristic of the converter stage of Figure 4.

Figure 6 shows a standard circuit block which may be employed for the detectors/comparators of Figures 1 and 3.

The converter comprises a series of stages connected in series, each stage including a full wave rectifier. The output terminals 3 and 4 of each rectifier are connected to the input terminals 1 and 2 of the rectifier of the next stage. A signal input current is provided to the first stage as i1 and −i1. Fixed currents i2 and i3 are introduced at the interconnections between first and second and second and third stages respectively for algebraic subtraction from the input current. Detectors D1, D2, D3 are provided

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to indicate the state of the currents at the input to each of the stages.

The input signal current i1 is arranged to have a range of plus and minus one unit of current. i2 is arranged to be fixed at one half unit of current and i3 is arranged to be fixed at one quarter unit of current.

Figure 2 shows how the currents change in the sections of the circuit at the input to the stages.

Detectors D1, D2, D3 are arranged to detect the point of crossing a zero current level of i1, i2 and i3 respectively. The detectors provide a logical output when the current is positive and a logical zero when the current is negative.

As i1 changes from −1 unit of current to plus one unit of current the detectors will change state and provide a digital indication of the amplitude of the input current i1.

The alternative form of converter shown in Figure 3 is to be preferred for some applications, particularly when a large number of stages are employed for high resolution and when small analogue currents are to be converted to digital form, as the current level in each stage is similar due to the provision of differential "buffer" amplifiers between each stage. Each stage comprises a current amplifier 10, a full wave bridge rectifier 11 and a detector or comparator 12 and has provision for feeding a fixed offset current into the bridge, equal in magnitude to one half the peak-to-peak full scale output current range.

The simplified circuit diagram of a single stage is shown in Figure 4. The amplifier 10 is formed as a balanced cascade differential amplifier from transistors TR1, 2, 3 and 4 with emitter load resistors R5 and R6 connected to a current source S1. The amplifier drives the bridge rectifier, formed by diodes D1, D2, D3, D4 directly and a bridge current offset is provided by unbalancing the inputs to the bases of TR1 and TR2 by suitable choice of resistors R1, R2, R3, R4. The stages each have two input terminals 21 and 22, and two output terminals 23 and 24 and operate with symmetrical, balanced input and output signal currents.

Current sources S2 and S3 form collector load circuits for the differential amplifier. Each of the sources S1, S2 and S3 are in the form of precision constant current transistor circuits and are arranged such that, the sum of the currents S2 and S3 is equal to the current S1. The values of R5 and R6 are chosen so that the current flowing through each of transistors TR1, TR2, TR3, TR4, when the bridge is balanced, is substantially larger e.g. at least five times than the maximum change of current through those transistors when the input current changes from maximum to zero.

All stages of th converter employ identical circuits but the polarity of the transistors and diodes is reversed in alternate stages to facilitate direct interconnection.

Considering the currents at one input and one output terminal only of one stage, the transfer characteristic is such that when the input current to one terminal is reduced from the maximum value +I, to ½I, the current at the corresponding output terminal changes from +I through ½I to zero. A further change of input from ½I to zero results in the output current changing from zero, through ½I, back to the initial value of +I. This transfer characteristic is shown in Figure 5.

The detectors 12 are arranged so as to detect the point of reversal of the bridge output current, and provide a logical one output when the current is flowing in one arm of the bridge, and a logical zero when it flows in the opposite arm. Due to the diode characteristics, a comparatively large voltage change occurs on TR3 and TR4 collectors at the reversal, so that the offset requirements for the detectors are easily met. Although Figure 1 shows a 3-stage and Figure 3 a two-stage Analogue to Digital converter, further stages may be added to improve the resolution. When a suitably scaled input signal is applied to the first stage of either arrangement, the logical outputs from the detectors provide a digital version of the input in a code known as Gray or Reflected Binary.

The standard block of Figure 6 may be any suitable current detector or comparator e.g. a differential switch or Schmitt trigger circuit.

The circuit is suitable for fabrication by integrated circuit or thin or thick film techniques.

WHAT WE CLAIM IS:—

1. An analogue to digital converter comprising a plurality of stages, each stage including a full wave rectifier having first and second input terminals and first and second output terminals, a detector connected between said first and second input terminals and in each stage except the first, a first and a second constant current source connected respectively to said first and second input terminals, whereby when the converter is connected to an analogue current, the analogue current flows in the full wave rectifier of the first stage between first and second stages, the respective detector providing a logic output when the current flows in one direction through the full wave rectifier and a logic zero when the current flows in the opposite direction through the full wave rectifier to differentiate between

an analogue current of greater r less than a predetermined level.

2. A converter as claimed in claim 1, wherein the constant current generators of each stage provide currents of magnitude one half of the magnitude of a predetermined maximum current which is fed to the stage, the current being subtracted from the input current, the magnitude of the currents from said first and second constant current generators for each stage subsequent to the second providing currents equal to one half the magnitude of the currents provided by the first and second constant current generators of the previous stage and first and second constant current generators of the second stage provide current equal to one half the maximum input current to the converter.

3. A converter as claimed in claim 1, wherein each stage is provided with a differential amplifier circuit the output terminals of which are connected to said first and second input terminals of the full wave rectifier and the input terminals of which are connected to the output terminals of the full wave rectifier of the previous stage, which amplifier is arranged to provide an output current from the output terminals of the full wave rectifier which varies linearly between a maximum stage input level, zero and back to maximum as the stage input current varies linearly between maximum and zero.

4. A converter as claimed in any one of claims 1 to 3 wherein the full wave rectifier is a diode bridge circuit.

5. A converter as claimed in any one of claims 1 to 4 wherein the detector is formed by a differential switch.

6. An analogue to digital converter substantially as herein described with reference to, and as illustrated in, the accompanying drawings.

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3 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1.

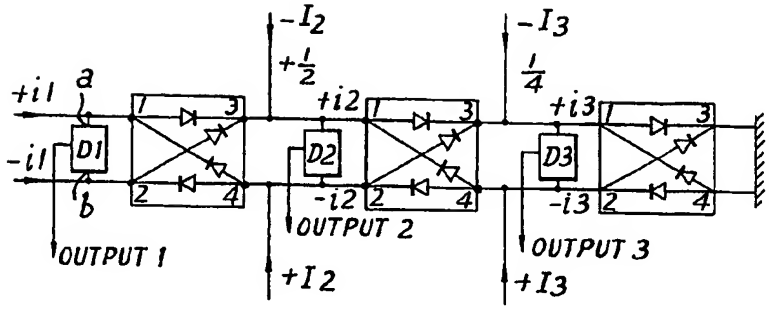


FIG. 2.

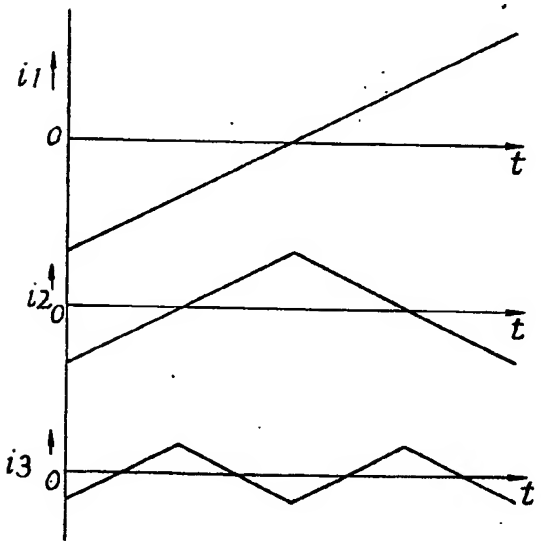


FIG. 3.

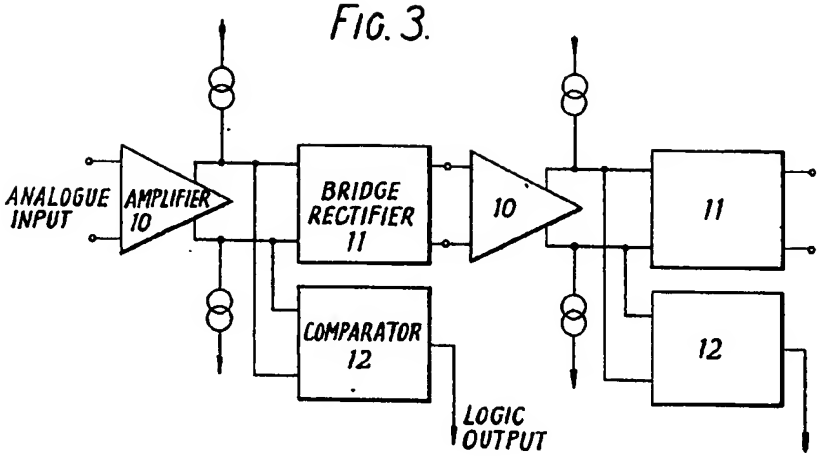

ANALOGUE INPUT
AMPLIFIER 10
BRIDGE RECTIFIER 11
10
11
COMPARATOR 12
12
LOGIC OUTPUT

FIG. 4.

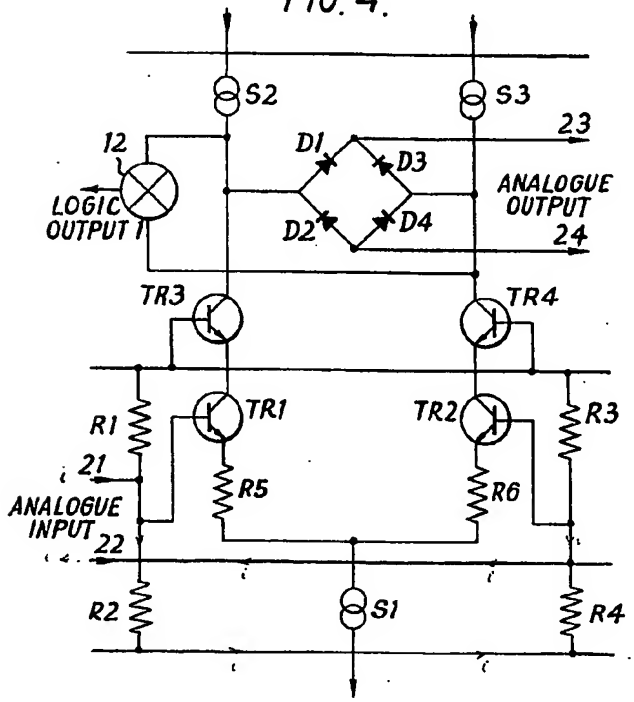

S2
S3
23
12
D1
D3
LOGIC OUTPUT
ANALOGUE OUTPUT
24
D2
D4
TR3
TR4
TR1
TR2
R1
R3
21
R5
R6
ANALOGUE INPUT
22
R2
S1
R4

FIG. 5.

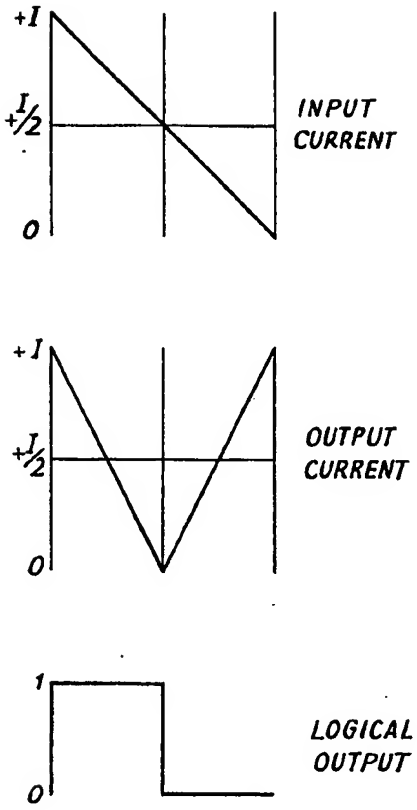
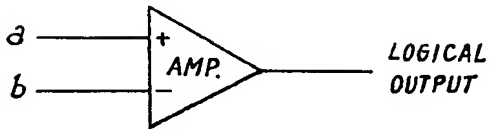

+I
I/2
0
INPUT CURRENT
+I
I/2
0
OUTPUT CURRENT
1
0
LOGICAL OUTPUT

FIG. 6.


a
b
+
AMP.
−
LOGICAL OUTPUT